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| 09/784,015 | 02/16/2001 | Frank Nico Lieven OpT Eynde | Q62388 | 1583 |

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| EXAMINER |
|---|
| PAREKH, NITIN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Applicati n No. | Applicant(s) | |
|---|---|---|---|
| | 09/784,015 | OP'T EYNDE ET AL. | |
| | Examiner | Art Unit | |
| | Nitin Parekh | 2811 | |

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2 and 4-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Pri rity under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 12-15, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al. (US Pat. 5786738) in view of Sholley et al. (US Pat. 6265774).

Regarding claim 1, Ikata et al. disclose a packaged integrated circuit (PIC- 32 in Fig. 2A/2B) comprising:

- a radio communication/radio frequency(RF) filter chip component/IC die/module (33a/33b in Fig. 2A and 2B), the die being directly connected by bonding wires (34 in Fig. 2B) to a high frequency/radio frequency antenna (RFA) interconnection patterns/circuits (37a-c in Fig. 2A) and RFA terminals (36a-36c in Fig. 2A)
- the IC die being included in the PIC, wherein the RFA interconnection patterns/circuits and terminals comprise a portion of the PIC and being excluded from the IC die (see Fig. 2B) or being on the exterior surface of the PIC

(Fig. 2A, 2B and 5; Col. 5, line 1- Col. 6, line 27; Col. 2-11).

Ikata et al. fail to teach the RFA interconnection patterns/circuits and terminals being the radio frequency antenna.

Sholley et al. teach conventional high frequency/RF packages where interconnection patterns and leads/terminals connecting a RF component serve/act as an antenna itself operating at full wave or half-wave picking up transmission or radiating energy as required by the circuit applications (Col. 1, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the RFA comprising interconnection patterns/circuits and terminals as taught by Sholley et al. so that the desired resonance frequency/impedance characteristics can be achieved and the transmission signal propagation can be improved in Ikata's PIC.

Regarding claim 2, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. further teach the PIC which houses the RF component and the RFA comprising terminals and metal object/wiring patterns being made of metals such as tungsten, copper, etc (Col. 6, line 57; Col. 7, line 5).

Regarding claim 5, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. further teach the RFA comprising planar metal patterns (37 a, b, c, etc. in Fig. 2A) being separated from the

ground/shield metal planes (GND planes in Fig. 2B) by insulating ceramic layers (32-1, 32-2, etc. in Fig. 2B; Col. 5 and 6).

Regarding claim 12, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. teach the PIC being the RF module/ceramic package.

Regarding claim 13, Ikata et al. disclose a packaged integrated circuit (PIC- 32 in Fig. 2A/2B) comprising:

- a radio communication/radio frequency(RF) filter chip component/IC die/module (33a/33b in Fig. 2A and 2B), the die being directly connected by bonding wires (34 in Fig. 2B) to a high frequency/ radio frequency antenna (RFA) interconnection patterns/circuits (37a-c in Fig. 2A) and RFA terminals (36a-36c in Fig. 2A)
- the IC die being included in the PIC, wherein the RFA interconnection patterns/circuits and terminals comprise a portion of the PIC and being excluded from the IC die (see Fig. 2B) or being on the exterior surface of the PIC
- the IC die being directly connected by bonding wires/metal wiring/wiring pattern including through holes/vias (see vias in Fig. 2B- not numerically referenced; Col. 5, line 2-36)

- the wiring being routed through the electrical ground/shield patterns/planes (GND lanes in Fig. 2B) interposed between the die and RFA interconnection patterns/circuits and terminals, and
- the PIC being hermetically sealed (Col. 5, line 16)

(Fig. 2A, 2B and 5; Col. 5, line 1- Col. 6, line 27; Col. 2-11).

Ikata et al. fail to teach the RFA interconnection patterns/circuits and terminals being the radio frequency antenna.

Sholley et al. teach conventional high frequency/RF packages where interconnection patterns and leads/terminals connecting a RF component serve/act as an antenna itself operating at full wave or half-wave picking up transmission or radiating energy as required by the circuit applications (Col. 1, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the RFA comprising interconnection patterns/circuits and terminals as taught by Sholley et al. so that the desired resonance frequency/impedance characteristics can be achieved and the transmission signal propagation can be improved in Ikata's PIC.

Regarding claim 14, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 13 above, wherein Ikata et al. further teach the PIC which houses the RF component and the RFA comprising terminals and metal object/wiring patterns being made of metals such as tungsten, copper, etc (Col. 6, line 57; Col. 7, line 5).

Regarding claim 15, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 13 above, wherein Ikata et al. further teach the RFA comprising planar metal patterns (37 a-c, etc. in Fig. 2A) being separated from the ground/shield metal planes (GND planes in Fig. 2B) by insulating ceramic layers (32-1, 32-2, etc. in Fig. 2B; Col. 5 and 6).

Regarding claim 26, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 13 above, wherein Ikata et al. teach the wiring connections comprising electrical ground/shield patterns/planes (see Fig. 2B).

Regarding claim 27, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, except the length of the wire being ¼ to ½ the wavelength of a transmitted or received radio signal.

Sholley et al. further teach using small dimensions for leads/wires serving as a full or one-half of the wavelengths of high frequency antenna (Col. 1, line 25-55).

Furthermore, determination of parameters and configuration of wiring such as wire thickness/length, pattern/layout of wiring layer, etc. with respect to the wavelength of transmitted signals in a high frequency/RF chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical resistance, noise reduction and signal propagation/performance.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the length of the wire being ¼ to ½ the wavelength of a transmitted or received radio signal as taught by Sholley et al. so that signal propagation and performance can be improved in Ikata et al's PIC.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al. (US Pat. 5786738) and Sholley et al. (US Pat. 6265774) as applied to claims 1 and 2 above, and further in view of Masahito (Japanese Pat. 08250913, IDS paper #3).

Regarding claim 4, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claims 1 and 2 above, except the RFA being disposed on a metal frame.

Masahito teaches forming/disposing a RFA on a conventional metal lead frame/terminal (203 in Fig. 13; Detailed Description pp. 1).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to dispose the RFA on a metal frame configuration as taught by

Masahito so that a wide range of external connection capabilities can be achieved in Ikata's PIC.

4. Claims 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al (US Pat. 5786738) and Sholley et al. (US Pat. 6265774) as applied to claims 1, 5, 13 and 15 above, and further in view of Masahito (Japanese Pat. 08250913, IDS paper #3), Koichi (Japanese Pat. 63181505, IDS paper #3) and Yoshikata (Japanese Pat. 06085530, IDS paper #3).

Regarding claims 6-8 and 16-18, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claims 1, 5, 13 and 15 above, except the metal pattern being a metal slot pattern or that comprising a first S-shaped slot or a second S-shaped slot which is rotated 90 degrees with respect to the first one respectively.

Ikata et al. further disclose forming maze-shape metal patterns by etching (Col. 6, line 3)

Koichi (Fig. 2; pp. 1-4) and Yoshitaka (Fig. 1; pp. 1-6) teach forming a RFA having slot patterns including S-shaped slot and strip-line configuration respectively with predetermined dimensions to achieve the desired resonance frequency/impedance characteristics.

Furthermore, selecting the parameters and configuration of wiring such as shape/size, number of layers, pattern/layout on each layer, wire thickness/length, etc. in a high frequency/RF chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical resistance, noise reduction and signal propagation/performance.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a RFA using a metal slot pattern consisting of a first S-shaped slot or a first slot and a second S-shaped slot which is rotated 90 degrees with respect to the first one as taught by Koichi and Yoshitaka so that the desired resonance frequency/impedance characteristics can be achieved and the transmission signal can be improved in Sholley et al. and Ikata's PIC.

5. Claims 9-11 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al. (US Pat. 5786738) and Sholley et al. (US Pat. 6265774) as applied to claims 1 and 13 above, and further in view of Houghton et al. (US Pat. 6282095).

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Regarding claims 9-11 and 23-25, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claims 1 and 13 above, except the PIC being a ball grid array (BGA), Quad Flat Pack (QFP) or Small Outline Package (SOP) respectively.

Houghton et al. teach using conventional packaging technologies such as a BGA, Small Outline Package (SOP), peripheral Quad Flat Pack (QFP), etc. in a RF module (Col. 5, line 15-25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the PIC being a BGA, QFP or SOP as taught by Houghton et al. so that a wide range of external connection capabilities can be configured in Ikata's PIC.

Regarding claims 19 and 20, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 13 above, except the plurality of vias being arranged around the periphery of the RFA and opposite to each other on the periphery of the RFA respectively.

Ikata et al. further teach through holes/vias (not numerically referenced in Fig. 2B) connecting the plurality of layers to provide the electrical connection with the RFA (Col. 5, line 18).

Houghton et al. teach the RF package/module having a heat slug/heat sink (60/74 in Fig. 1) serving as a RFA where plurality of vias/internal signals (63/65 in Fig. 1) are arranged around the periphery of the RFA to provide the desired external connection capability around the peripheral area of top external surface of the package (Col. 5, line 45; Col. 4, line 65- Col. 5, line 48; Col. 2, lines 40-60).

Furthermore, selecting the parameters of wiring such as via size, number, location/pattern, wire thickness/length, etc. in a high frequency/high power chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical resistance, noise reduction and the module performance.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select an arrangement of the plurality of vias being around the periphery or having two vias being opposite each other as taught by Houghton et al. so that signal propagation, routing and performance can be improved in Sholley et al. and Ikata et al's PIC.

6. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al. (US Pat. 5786738) and Sholley et al. (US Pat. 6265774) as applied to claim 13 above, and further in view of Masahito (Japanese Pat. 08250913, IDS paper #3) and Moskowitz et al. (US Pat. 5528222).

Regarding claims 21 and 22, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 13 above, except the RFA being disposed on a metal frame of the IPC and the IPC encapsulating the shield and the die.

Masahito teaches forming/disposing a RFA on a conventional metal lead frame/terminal (203 in Fig. 13; Detailed Description pp. 1).

Moskowitz et al. teach using a conventional encapsulation/resin sealing of components including a chip/die, bonding wire, etc. for a RF package (130 in Fig. 1A/1B; Col. 2) to provide added protection.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the RFA being disposed on a metal frame of the IPC as taught by Masahito and the IPC encapsulating the shield and the die as taught by Moskowitz et al. so that the desired protection/sealing for the internal components can be provided in Sholley et al. and Ikata's PIC.

***Response to Arguments***

7. Applicant's arguments filed on 06-06-03 have been fully considered but they are not persuasive.

A. Applicant's arguments with respect to claims 1, 2 and 4-27 with respect to the limitations: a) the RFA interconnection patterns and terminals serving as the RFA itself, b) an arrangement of a plurality of via holes and c) the PIC encapsulating the shield and the die, have been considered but are moot in view of the new ground(s) of rejection.

B. Applicant contends that Ikata et al. do not teach the RFA being excluded from the die.

However, Fig. 2B in Ikata et al. clearly shows the RFA (37a-37c and 36a-36c) being separate/excluded from the dice 33a/33b and the dice being included in the PIC.

C. Applicant contends that Ikata et al. do not teach the RFA being a portion of the package/ICP.

However, Fig. 2B in Ikata et al. clearly shows the RFA (37a-37c and 36a-36c) being the portion of the PIC 32.

D. Applicant contends that Masahito does not teach the RFA being disposed on a metal frame of the IPC.

However, Fig. 13 in Masahito shows the die/chip and the circuitry having the RFA (201 in Fig. 13) being disposed in the conventional PIC 200 and being connected to the metal lead frame 203.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

09-13-03

Tom Thomas

TOM THOMAS
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